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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,190	06/07/2000	Yoshiaki Shiota	067183/0186	8859

22428 7590 03/30/2005

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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/588,190	SHIOTA, YOSHIAKI	
	Examiner	Art Unit	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim 9 has been examined.

This action is made **Non-FINAL**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 6,202,090 of Simone in further view of Japanese Patent No. 02226432 of Nakamura and Japanese Patent No. 01311792 of Fukada.

In regards to claim 9, Simone discloses a fault management system for a switching equipment (see column 2 lines 58-62) which includes a circuit section to an external terminal equipment over a communication circuit, a switch section for communicating data with said circuit section, and a processor (see figure 1 item 14 and column 2 lines 60-65) for performing setting and control of said circuit section, protocol processing of a transmission/reception packet and other necessary processing over a processing bus, comprising:

a fault detection section. Simone states a reset occur for any one of a variety of software and hardware faults (see column 4 lines 7-8)

a concentrated fault management section connected to said processor bus for a supervising the normality of said processor bus and signaling, if a fault notification is received, a reset signal to said processor and said circuit section without intervention of said processor bus so that data in a data link layer or an upper layer may not flow. Simone discloses an internal bus and further states a variety of software and hardware faults, such as a bus error, causes a shut down routine, indicating supervising the normality of the processor bus and signaling (see column 4 lines 7-13). Furthermore, the shutdown routine would result in a reset, indicating a reset signal to said processor and said circuit section so that data in a data link layer or an upper layer may not flow from said processor or said circuit section. Also, Simone discloses a reset signal without intervention of said processor bus because there is no indication of the processor bus interfering or intervening with a shutdown routine or reset.

issuing a notification of occurrence of a fault to a central control section connected to an external console. Simone states the compressed core file can be accessed through a device (or external console) coupled to auxiliary port (see column 5 lines 34-37). The auxiliary port may constitute as a central control section because applicant discloses the central control section as being connected to external console and sending notification to the console when a fault occurs, which the auxiliary port does. The sending of the core compress file constitutes a notification of occurrence of a fault. If compress file was not received, no fault would of occurred.

However, Simone fails to disclose:

a clock fault detection section for detecting whether or not supply of a clock signal from an oscillator for supplying the clock signal to said processor is interrupted, and

continuously signal a reset signal.

Nakamura discloses a clock fault detection circuit, which detects abnormalities or interrupts in a clock supplied from a clock distribution circuit to processors through a clock signal (see abstract), indicating a clock fault detection section for detecting whether or not supply of a clock signal from an oscillator for supplying the clock signal to said processor is interrupted.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Simone to include a clock fault detection section, which detects whether or not supply of a clock signal of an oscillator which supplies the clock signal to said processor is interrupted, as per teaching of Nakamura. A person of ordinary skill in the art would have been motivated to make the modification to Simone because Simone discloses resets occur for any one of a variety of software and hardware faults, and clock faults constitute has software and hardware faults and having clock fault detection section, would indicate faults as a result of interrupts in clock signal to processor.

Furthermore, Fukada discloses transmitting a continuous signal, which causes the CPU to restart, indicating continuously signaling a reset signal (see abstract)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Simone to continuously signal a reset signal. A person of ordinary skill in the art would have been motivated to make the modification to Simone because Simone discloses resetting for any one of a variety of hardware and software faults, and continuously signaling a reset, as per teaching of Fukada, would assure resetting or shutdown to occur.

Response to Arguments

Applicant's arguments filed March 18, 2005 have been fully considered but they are not deemed to be persuasive.

In response to applicant's argument that argues: "However, neither Simone, Nakamura nor Fukada taken either singly or in combination disclose or make obvious applicant's invention as recited in amended claim 9. The limitation of 'contintously signaling, if a fault notification of the interruption of the supply of the clock signal is received from said clock fault detection section, a reset signal to said processor and said circuit section without intervention of said processor bus' is simply not disclosed in the prior art references," examiner respectfully disagrees.

Since there is no indication of the processor bus interfering or intervening with a shutdown routine or reset, Simone discloses a reset signal without intervention of said processor bus as claimed. Examiner maintains his rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emerson Puente
3/25/05

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